UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/785,122 | 02/24/2004 | Frank L. Hall | 5165.1US (01-0947.01/US) | 1653 |

24247 7590 11/18/2005

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

| EXAMINER | |
|---|---|
| DIAZ, JOSE R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/785,122 | HALL ET AL. | |
| | Examiner | Art Unit | |
| | José R. Díaz | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *4-6,10,18,22-24,28 and 36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-9,11-17,19-21,25-27,29-35 and 3742* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/04, 4/20/04*, 01/18/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Species II, e.g. Figure 5, in the reply filed on August 29, 2005 is acknowledged.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 11, 14-17, 19-21, 29, 32-35, 37-38, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden (US Pat. No. 5,719,440) in view Tummala et al., Microelectronics Packaging Handbook Semiconductor Packaging Part II, 2nd Ed., Chapman and Hall, 1997, pages 25-26, 42-44, 91-93, 887-890.

Regarding claims 1, 19 and 37, Moden teaches a semiconductor assembly comprising:

a carrier substrate (18) having conductive pads (39) exposed on a surface (24) thereof [see fig. 3];

a semiconductor substrate (12) adjacent the carrier substrate and having an active surface (14) and a back surface (opposite "top" surface), the active surface (14) having bond pads (38) exposed thereon [see fig. 3];

a plurality of wire bonds (134) extending between the bond pads of the semiconductor substrate and the conductive pads of the carrier substrate [Fig. 3]; and

a plurality of spaced[1] adhesive elements (40) disposed in an area of overlap between a face of the carrier substrate (20) and an opposing surface (14) of the semiconductor substrate [see fig. 3]; and

a volume of filler material (44) disposed between adjacent spaced adhesive elements (40) in the area of overlap and bonding the semiconductor substrate (12) to the carrier substrate (18) [see fig. 3].

However, Moden is silent with respect to using a dielectric material as the filler material. Tummala et al. teaches the use of a dielectric material as encapsulation or sealant material (see fig. 14-5) and coupling the semiconductor assembly to at least one processor device , input device and output device (Section 7.2.2.1 and fig. 7-20).

Moden and Tummala et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a filler material comprising a dielectric material. The motivation for doing so, as is taught by Tummala et al., is to protect the electronic components from adverse environment and thereby increase their long-term reliability (page II-887). Therefore, it would have been obvious to combine Tummala et al. with Moden to obtain the invention of claims 1-3, 11, 14-17, 19-21, 29, 32-35, 37-38, and 40-41.

[1] Consider adhesive elements (40) spaced by aperture or via (42).

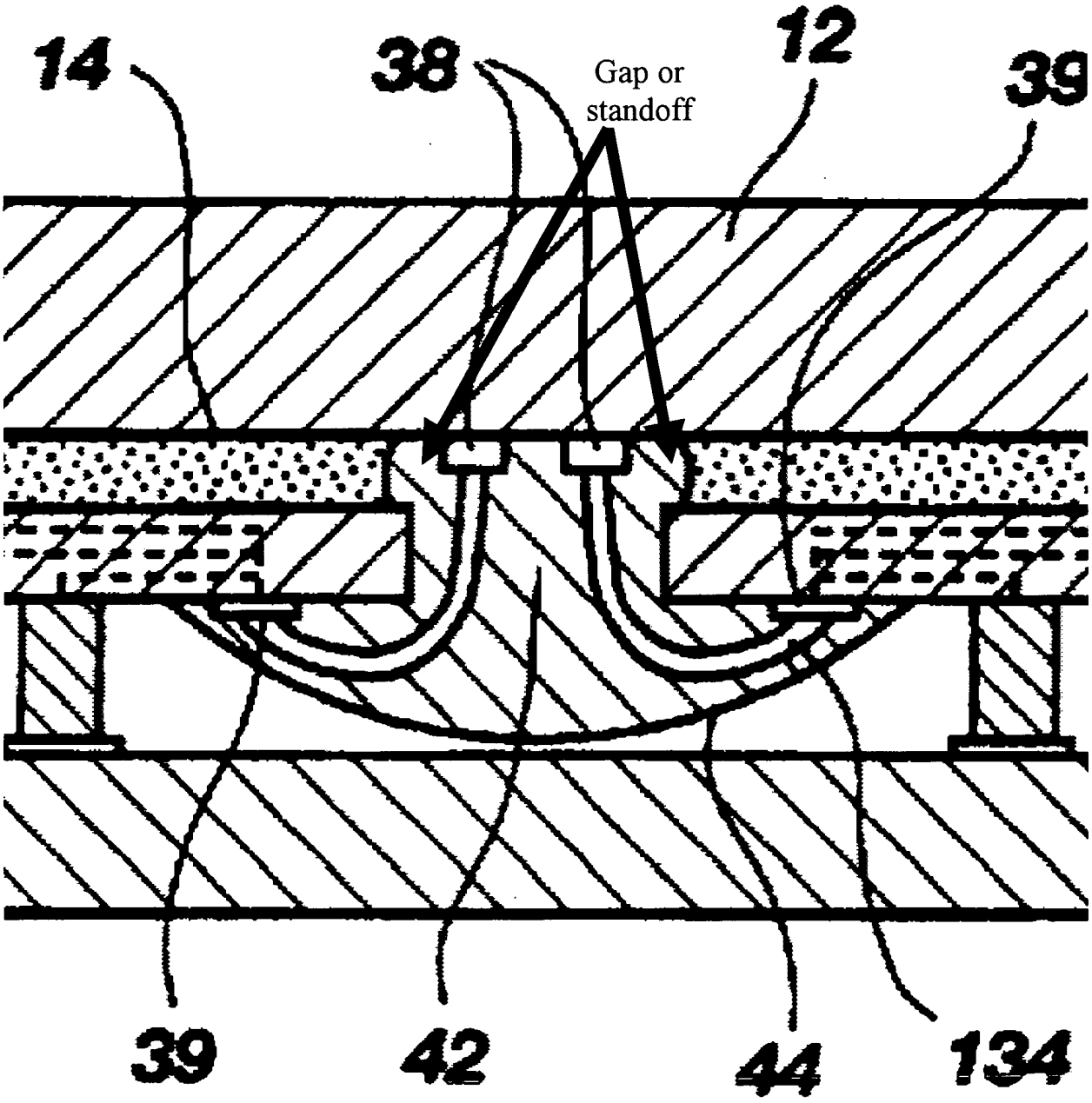
Regarding claims 2, 20 and 40, Moden further teaches that the carrier substrate (18) comprises a first surface (20), a second surface (24) and an opening (42) extending through the carrier substrate (18) therebetween [see fig. 3], the second surface (24) having the conductive pads (39) exposed thereon [fig. 3], the semiconductor substrate (12) located over the first surface (20) of the carrier substrate (18) so that the bond pads (38) are exposed through the opening (42) and the plurality of wire bonds (134) extends through the opening (42) between the bond pads (38) and the conductive pads (39) [see fig. 3].

Regarding claims 3 and 21, Moden further teaches that the plurality of spaced adhesive elements (40) comprises a substantially symmetrical adhesive element arrangement (compare the adhesive elements located at each side of the aperture (42), both having similar size and shape) [see fig. 3].

Regarding claims 11, 29, 38 and 41, Moden further teaches that the dielectric filler material (44) coats or encapsulates at least portions of at least some of the plurality of wire bonds (134) [see fig. 3].

Regarding claims 14 and 32, Moden further teaches that the dielectric filler material (44) substantially fills a standoff (consider the gap or standoff shown in figure 3, attached below) between the semiconductor substrate (12) and the carrier substrate (18).

Regarding claims 15 and 33, Moden further teaches that the plurality of spaced adhesive elements (40) comprises a volume of adhesive or sealing adhesive (col. 5, line 3).




Regarding claims 16 and 34, Moden further teaches that the semiconductor substrate comprises one semiconductor dice (12) [see fig. 3 and col. 3, line 12].

Regarding claims 17 and 35, Tummala et al. teaches a carrier substrate comprising at least a ceramic material (section 7.5.8).

4. Claims 7-9 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden (US Pat. No. 5,719,440) in view Tummala et al., Microelectronics Packaging Handbook Semiconductor Packaging Part II, 2nd Ed., Chapman and Hall, 1997, pages 25-26, 42-44, 91-93, 888-890; and further in view of Jiang (US Pat. No. 6,359,334 B1).

Regarding claims 7-9 and 25-27, a further difference between the prior art references and the claimed invention is the further limitation of elongated pads positioned adjacent the opening and extended parallel to the opening. Jiang teaches elongated adhesive pads (10A, 10B) located parallel to opening (26) [see fig. 2].

Jiang, Moden and Tummala et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further include elongated adhesive pads located parallel to the opening. The motivation for further doing so, as is taught by Jiang, is to dissipate any excessive heat generated by the integrated circuit (col. 2, lines 60-62). Therefore, it would have been obvious to further combine Jiang with Tummala et al. and Moden to obtain the invention of claims 7-9 and 25-27.

5. Claims 12-13, 30-31, 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden (US Pat. No. 5,719,440) in view Tummala et al.,

Microelectronics Packaging Handbook Semiconductor Packaging Part II, 2nd Ed., Chapman and Hall, 1997, pages 25-26, 42-44, 91-93, 888-890; and further in view of Mine et al. (US Pat. No. 5,561,329).

Regarding claims 12-13, 30-31, 39 and 42, a further difference between the prior art references and the claimed invention is the further limitation of a volume of dielectric encapsulation material extending over at least exposed portions of wire bonds having portions coated or encapsulated by the dielectric filler material. Mine et al. teaches a composition for protecting semiconductor devices consisting of a filler material (6) and resin (7) extending over at least exposed portions of wire bonds having portions coated or encapsulated by the dielectric filler material [see fig. 1].

Mine et al., Moden and Tummala et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further include a volume of dielectric encapsulation material extending over at least exposed portions of wire bonds having portions coated or encapsulated by the dielectric filler material. The motivation for further doing so, as is taught by Mine et al., is protecting semiconductor elements which afford highly moisture-resistant and highly heat resistant semiconductor devices (col. 1, lines 37-42). Therefore, it would have been obvious to further combine Mine et al. with Tummala et al. and Moden to obtain the invention of claims 12-13, 30-31, 39 and 42.

## *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Froebel et al. (US Pat. No. 5,858,600) discloses an encapsulated device having a dual composition (layers 28 and 32) [see fig. 3]; and Corbett et al. (US Pat. No. 5,548,160) and Grigg et al. (US Pat. NO. 5,840,598) disclose elongated adhesive pads (18) and (40), respectively.

## *Correspondence*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

José R. Díaz
Examiner
Art Unit 2815